second conductivity type collector region being provided in the second main surface of the semiconductor substrate;

(g) a first conductivity type field stop region being of the same conductivity type as the first conductivity type, provided on the second main surface side in the drift region so as to contact the second conductivity type collector region, the first conductivity type field stop region being higher than the drift region in impurity concentration; and

(h) a second conductivity type high-concentration collector contact region being of the same conductivity type as the second conductivity type collector region, provided on the metal collector electrode side in the second conductivity type collector region, the second conductivity type high-concentration collector contact region being more higher in impurity concentration,

wherein the each linear unit cell area comprises:

(d1) a linear active cell area provided from over the first main surface in the drift region to the inside thereof;

(d2) a pair of linear trench gate electrodes lying within a pair of trenches provided in the surface of the first main surface so as to sandwich the linear active cell area therebetween from both sides as seen on a plane basis;

(d3) a second conductivity type body region of a conductivity type opposite to the first conductivity type, the second conductivity type body region being provided in a surface region on the first main surface side, of the drift region;

(d4) linear inactive cell areas provided adjacent to each other on both sides so as to sandwich the linear active cell area therebetween from both sides thereof on a plane basis with the pair of linear trench gate electrodes as boundaries;

(d5) a first conductivity type emitter region of the same conductivity type as the first conductivity type, the first conductivity type emitter region being provided in a surface region on the first main surface side, of the second conductivity type body region in the linear active cell area; and

(d6) a second conductivity type floating region of a conductivity type opposite to the first conductivity type, the second conductivity type floating region being provided approximately over a whole area of the surface region on the first main surface side in the linear inactive cell area,

wherein the second conductivity type floating region covers lower ends of the pair of trenches and is deeper than the pair of trenches in depth.

15. The IE-type trench gate IGBT according to claim **14**, wherein each of the linear unit cell areas further comprises:

(d7) a first conductivity type hole barrier region being of the same conductivity type as the first conductivity type, provided in the drift region lying underneath the second conductive type body region in the linear active cell area, the first conductivity type hole barrier region being higher than the drift region and lower than the first conductivity type emitter region in impurity concentration.

16. An IE-type trench gate IGBT comprising:

(a) a semiconductor substrate comprising a first main surface and a second main surface;

(b) a drift region of a first conductivity type provided within the semiconductor substrate;

(c) a cell area provided over the first main surface; and

(d) a number of linear unit cell areas provided within the cell area as seen on a plane basis;

wherein the each linear unit cell area comprises:

(d1) a linear active cell area provided from over the first main surface in the drift region to the inside thereof;

(d2) a pair of linear trench gate electrodes lying within a pair of trenches provided in the surface of the first main surface so as to sandwich the linear active cell area therebetween from both sides as seen on a plane basis;

(d3) a second conductivity type body region of a conductivity type opposite to the first conductivity type, the second conductivity type body region being provided in a surface region on the first main surface side, of the drift region;

(d4) linear inactive cell areas provided adjacent to each other on both sides so as to sandwich the linear active cell area therebetween from both sides thereof on a plane basis with the pair of linear trench gate electrodes as boundaries;

(d5) a first conductivity type emitter region of the same conductivity type as the first conductivity type, the first conductivity type emitter region being provided in a surface region on the first main surface side, of the second conductivity type body region in the linear active cell area; and

(d6) a second conductivity type floating region of a conductivity type opposite to the first conductivity type, the second conductivity type floating region being provided approximately over a whole area of the surface region on the first main surface side in the linear inactive cell area,

wherein further the second conductivity type floating region covers lower ends of the pair of trenches and is deeper than the pair of trenches in depth, and

wherein the IE-type trench gate IGBT further comprises:

(e) a metal emitter electrode provided over the first main surface of the semiconductor substrate;

(f) linear dummy cell areas each provided on the outermost side of the cell area, the linear dummy cell area extending in the same direction as the linear active cell area and comprising a contact portion with the metal emitter electrode; and

(g) a second conductivity type cell peripheral junction area being a conductivity type opposite to the first conductivity type, provided outside each linear dummy cell area so as to surround the periphery of the cell area as seen on a plane basis in the surface region on the first main surface side in the drift region, the second conductivity type cell peripheral junction area comprising a contact portion with the metal emitter electrode.

17. The IE-type trench gate IGBT according to claim **16**, wherein the linear dummy cell area comprises the same structure as the linear active cell area except that the first conductivity type emitter region is not provided therein.

18. The IE-type trench gate IGBT according to claim **16**, wherein the second conductivity type cell peripheral junction area extends to the inside of the linear dummy cell area.

19. The IE-type trench gate IGBT according to claim **16**, wherein each of the linear unit cell areas further comprises:

(d7) a first conductivity type hole barrier region being of the same conductivity type as the first conductivity type, provided in the drift region lying underneath the second conductivity type body region in the linear active cell area, the first conductivity type hole barrier region being